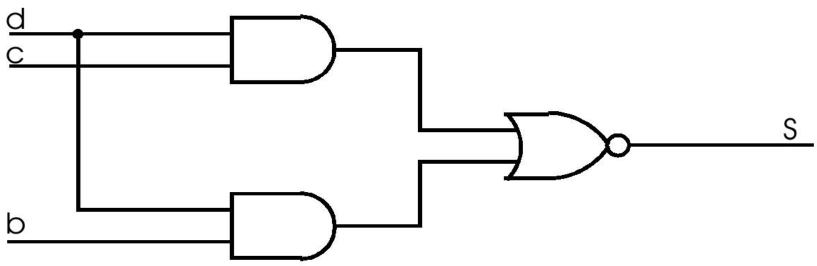
Exercises Unit 3: Combinational Systems

1. Analyse the following circuit obtaining the mathematical function S, the truth table and the two canonical forms of S



2. Express in Minterms and Maxterms the following functions:

   a)- F(c,b,a)= $\overline{((c+\bar{b})\cdot(\bar{c}+b+a+c\cdot b))}$

   b)- F(d,c,b,a)= $(d+\bar{b})\cdot(\bar{c}+b+\bar{a})$

3. Express in Minterms the following function:

   – F(a,b,c)= $a\cdot b+c+a\cdot\bar{c}+\bar{a}\cdot b\cdot c$

4. Simplify the following functions using Karnaugh:

   a)- F(d,c,b,a) = $\sum(0,1,4,5,6,8,9,13,14)$

   b)- F(d,c,b,a) = $\sum(0,1,2,4,5,8,10)$

   c)- F(d,c,b,a) = $\sum(0,1,3,4,5,7,8,9,14,15)$

   d)- F(d,c,b,a) = $\sum(1,2,3,5,6,7,8,9,10,11,14)$

5. Simplify the following functions using Boolean algebra and Karnaugh

   F(d,c,b,a)= $\sum$ (0,2,5,7,8,10,13,15)

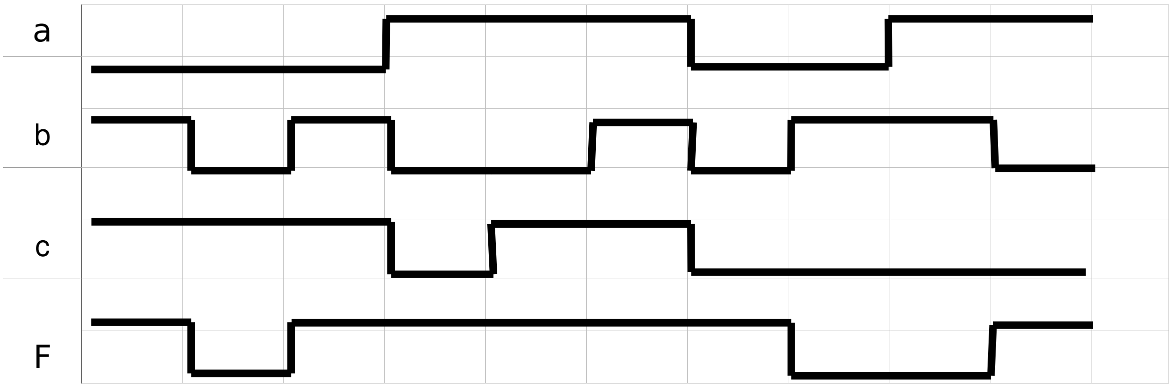
6. Design a circuit that implements the following functions:

   a)- $F1(d,c,b,a)= \sum (0,1,4,5,6,8,9,13,14)$ (same as 4.a)

   b)- $F2(d,c,b,a)= \sum (0,1,2,4,5,8,10,13,14)$

   c)- Design F1 using only NAND gates and F2 using only NOR gates

7. With the information of the signals a, b, c (inputs) and F (output) shown in the following time diagram, obtain the simplified expression of F using the known methods (Boolean algebra and Karnaugh)



8. Design a 3 to 8 decoder to be connected to a 7-segment display that shows the decimal value of the 3-bits binary input (design one circuit for each one of the seven segments)

9. Design a circuit that determines whether a 4-bits input binary number represents a BCD number.

10. Design a circuit that adds two BCD numbers and gives the result in 5-bits binary code. You can use BCD-adders, 4-bits adders and the necessary logical gates.

11. Given two 2-bits natural numbers, A(a2 A1) and B (b2 b1), design a circuit that computes the absolute value of their difference |A-B|

12. Design a circuit that adds two 2-bits natural numbers, A(a2 A1) and B(b2 b1), providing a 3-bits output

13. a) Design a circuit that compares two 2-bits natural numbers A(a2 A1) and B(b2 b1) providing 3 outputs (S3 S2 S1) such that

   - S1 = 1 if A > B and 0 otherwise
   - S2 = 1 if A = B and 0 otherwise
   - S3 = 1 if A < B and 0 otherwise

   b)- Obtain S2 as function of S1 and S3

14. Using multiplexers and logical gates, integrate the previous three circuits (exercises 11, 12 and 13) in a unique combinational circuit with two inputs, A(a2 A1) and B (b2 b1), and 3 outputs (S3 S2 S1). It will include as well two control inputs, C1 and C2, that will select what the circuit does:

   - If C2 =0 and C1 = 0 → Output must be S = 111
   - If C2 =1 and C1 = 0 → Output S will contain A+B
   - If C2 =0 and C1 = 1 → Output S will contain the comparison of A and B
   - If C2 =1 and C1 = 1 → Output must be |A-B|

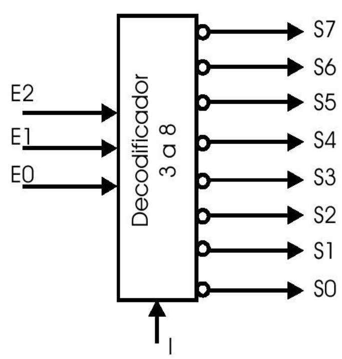
15. Design a circuit with a 4-bit input X(d,c,b,a) that performs the following operations:

   - If X>9 an output S1 is activated to switch a red light on
   - If X<9 an output S2 is activated to switch a green light on
   - If X=9 an output S2 is activated to switch a yellow light on

16. Design a circuit with a 8-bit input that indicates whether there are an even or odd number of "1" in the input.

17. Using 4-bits comparators 7485 design a 32-bits comparator

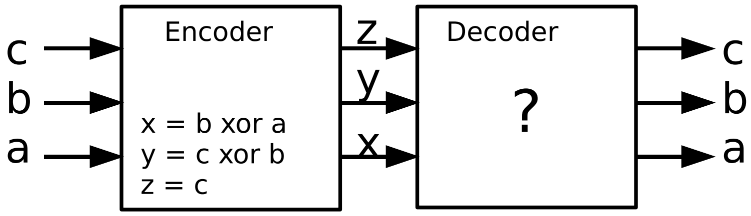
18. Design a 4 to 16 decoder using 3 to 8 decoders like the one in the figure



19. Design a circuit that converts BCD code to BCD with 3-excess

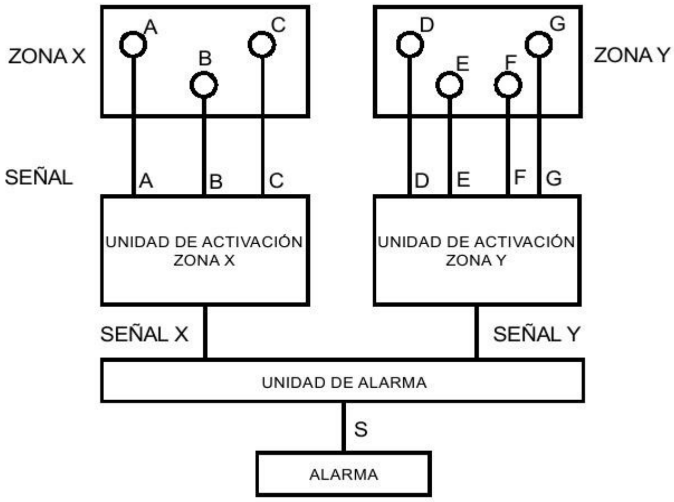
20. Design a decoder to visualize 3-bit binary numbers in a 7-segment display

21. An encoder codifies its inputs (c,b,a) into outputs (z,y,x) according to the equations in the figure



- Design a decoder that provides the initial input (c,b,a) from encoder's output (z,y,x)

22. A bank wants to install an alarm system with movement sensors. There are two security zones X and Y and the alarm must be triggered whenever X or Y are triggered. Zone X have 3 sensors (A,B,C) while zone Y possess 4 (D,E,F,G). To prevent false alarms produced by a single sensor activation, the alarm in each zone will must be triggered when at least two sensors activates simultaneously.



a) Design the alarm system

b) Rob the bank

De-Morgan Laws exercises

Simplify

1- $\overline{(\overline{(A+B\overline{\overline{C}})}+D\overline{(E+\overline{\overline{F}})})}$

2- $\overline{((A+B+C)D)}$

3- $\overline{(ABC+DFE)}$

4- $\overline{(A\overline{B}+\overline{C}D+EF)}$

5- $\overline{(\overline{ABC}+D+E)}$

6- $\overline{(\overline{(A+B)}+\overline{C})}$

7- $\overline{(\overline{A}+B+CD)}$

8- $\overline{((A+B)\overline{C}\overline{D}+E+\overline{F})}$

9- $\overline{(\overline{A}B(C+\overline{D})+E)}$

Boole Algebra exercises

Simplfy

	Expresssion	***Solution***
1-	$AB+A(B+C)+B(B+C)$	$B+AC$
2-	$A\overline{B}+A\overline{(B+C)}+B\overline{(B+C)}$	$A\overline{B}$
3-	$(A\overline{B}(C+BD)+\overline{A}\overline{B})C$	$\overline{B}C$
4-	$CD[AB(C+\overline{BD})+\overline{AB}]$	CD
5-	$\overline{A}BC+A\overline{B}\overline{C}+\overline{A}\overline{B}\overline{C}+A\overline{B}C+ABC$	$BC+A\overline{B}+\overline{C}\overline{B}$
6-	$AB\overline{C}+\overline{A}\overline{B}C+\overline{A}BC+\overline{A}\overline{B}\overline{C}$	$AB\overline{C}+\overline{A}C+\overline{A}\overline{B}$
7-	$\overline{(AB+AC)}+\overline{A}\overline{B}C$	$\overline{A}+\overline{B}\overline{C}$
8-	$\overline{AB}+\overline{AC}+\overline{A}\overline{B}\overline{C}$	$\overline{A}+\overline{B}+\overline{C}$