## ExERCISES OF

Fundamentals of computer technology

Unit 5. MEMORY SYSTEM

Most of the exercises in this units deal with installing memory chips in a computer to increase its capacity, either in number of available addresses, in word size, or both.

## Increasing memory capacity in number of addresses.

Example: In a CPU with an address bus of 14 bits, you are required to install a memory of 16 Kx 8 using chips of $8 \mathrm{Kx8}$. Design the memory system.
-Check that the required amount of memory can be addressed with 14 bits: $\quad 2^{14}=16 \mathrm{~K}$ -Calculate how many 8 Kx 8 chips are needed: $16 \mathrm{~K} / 8 \mathrm{~K} * 8 / 8=2$ * $1 \rightarrow 2$ chips of 8 Kx 8 -Scheme of the memory map:

| 0 | Módulo 0 de 8 Kx 8 |
| ---: | :--- |
| $8 \mathrm{~K}-1$ |  |
| 8 K | Módulo 0 de 8 Kx 8 |

Calculate addresses in each chip. As chips are of 8 K we need the least 13 significant bits $A_{12}-A_{0}$ to select an address in each of them ( $2^{13}=8 \mathrm{~K}$ ). The most significant bit $A_{13}$ will be used to select the chip with the CS input. Both will share the same data bus with 8 lines. The memory map and the system design are

| $\mathrm{A}_{13}$ | $\mathrm{~A}_{12}$ | $\mathrm{~A}_{11}$ | $\mathrm{~A}_{10}$ | $\mathrm{~A}_{9}$ | $\mathrm{~A}_{8}$ | $\mathrm{~A}_{7}$ | $\mathrm{~A}_{6}$ | $\mathrm{~A}_{5}$ | $\mathrm{~A}_{4}$ | $\mathrm{~A}_{3}$ | $\mathrm{~A}_{2}$ | $\mathrm{~A}_{1}$ | $\mathrm{~A}_{0}$ | Módulo |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :---: |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Módulo |
|  | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | 1 |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Módulo |  |
|  | 0 | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | 0 |



## Increasing memory capacity in word size:

Example: In a CPU with an address bus of 14 bits, you are required to install a memory of $16 \mathrm{Kx16}$ using chips of 8 Kx 8 . Design the memory system.
-Check that the required amount of memory can be addressed with 14 bits: $\quad 2^{14}=16 \mathrm{~K}$ -Calc. how many 8 Kx 8 chips are needed: $16 \mathrm{~K} / 16 \mathrm{~K}$ * $16 / 8=1$ * $2 \rightarrow 2$ chips of 16 Kx 8

Now the CPU accesses the same address in both chips at the same time, providing each of them half of the total 16 bits to be sent to the data bus when reading a position. The system design is now


Increasing memory capacity in number of addresses and in word size
In the following exercises the two cases shown above can be combined to increase the amount of available memory both in number of addresses and in word size.

## EXERCISES UNIT 5

1. In a CPU with 8 bits in the data bus and 10 bits in the address bus it is required to install two memory chips of $256 \times 8$. One must be in the lowest part of the map (ie. it must contain the first 256 addresses), and the other one in the highest part. Design the memory system.
2. In the computing system shown in the figure it is required that the 8 Kx 8 memory chip stores the lowest addresses in the map. Design the circuit to connect the necessary lines of the address bus to the chip select of the memory.

3. In the memory system shown in the figure, calculate the addresses that memory chips M1 and M2 store.

4. In a CPU with 16 bits in the data bus and 20 bits in the address bus it is required to install a memory system with the following characteristics:

- 256 Kwords ( $256 \mathrm{~K} \times 16$ ) of ROM memory.
- 512 Kwords ( $512 \mathrm{~K} \times 16$ ) of RAM memory.

Design the memory system allocating RAM memory in the lowest part of the map followed by ROM in the next positions. Use the minimum number of the following available chips

| ROM chips | RAM chips |
| :---: | :---: |
| $64 \mathrm{~K} \times 8$ | $128 \mathrm{~K} \times 1$ |
| $128 \mathrm{~K} \times 1$ | $256 \mathrm{~K} \times 8$ |
| $128 \mathrm{~K} \times 8$ |  |

5. In a CPU with 16 bits in the data bus and 20 bits in the address bus it is required to install a memory system with the following characteristics:

- 256 Kwords ( 256 K x 16) of ROM memory.
- 512 Kwords ( $512 \mathrm{~K} \times 16$ ) of RAM memory.

Design the memory system allocating RAM memory in the lowest addresses of the map and ROM in the highest ones. Use the minimum number of the following available chips:

| ROM chips | RAM chips |
| :---: | :---: |
| $64 \mathrm{~K} \times 8$ | $128 \mathrm{~K} \times 1$ |
| $128 \mathrm{~K} \times 1$ | $256 \mathrm{~K} \times 8$ |
| $128 \mathrm{~K} \times 16$ | $256 \mathrm{~K} \times 16$ |

6. In the CPU shown in the figure it is required to install a memory system with the following characteristics:

- 128 Kwords (128K x 16) of ROM memory
- 768 Kwords ( $640 \mathrm{~K} \times 16$ ) of RAM memory.


Design the memory system allocating RAM memory in the lowest addresses of the map and ROM in the highest ones. Use the minimum number of the following available chips:

| ROM chips | RAM chips |
| :---: | :---: |
| $64 \mathrm{k} \times 8$ | $128 \mathrm{k} \times 1$ |
| $128 \mathrm{k} \times 1$ | $256 \mathrm{k} \times 8$ |
| $128 \mathrm{k} \times 16$ | $256 \mathrm{k} \times 16$ |

7. In a CPU with 16 bits in the data bus and 16 bits in the address bus it is required to install 16 Kwords of RAM memory and 8 Kwords of EPROM memory. The following chips are available:


The address range for each type of memory must be:

|  | Firs address | Last address |
| :--- | :---: | :---: |
| RAM | 2000 h | 5FFFh |
| EPROM | 8000 h | $9 F F F h$ |

a) Design the memory system using the necessary logic gates
b) Design the memory system using the 3 to 8 decoder 74138 of the figure

|  |  |  |  |  | Inputs |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Enable |  | ele |  |  |  |  |  |  |  |  |  |
|  |  |  |  | G1 | G2 (Note 1) | C | B | A | YO | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
|  |  |  |  | X | H | X | X | X | H | H | H | H | H | H | H | H |
| 1 | A | Y0 | 0-15 | L | X | X | X | X | H | H | H | H | H | H | H | H |
| 2 | B | Y1 | $1-\frac{14}{13}$ | H | L | L | L | L | L | H | H | H | H | H | H | H |
| 3 | C | Y2 | O-13 | H | L | L | L | L | H | H | H | H | H | H | H | H H |
|  |  | Y3 | $0-12$ | H | L | L | L | H | H | L | H | H | H | H | H | H |
| 6 |  | Y4 | O-11 | H | L | L | H | L | H | H | L | H | H | H | H | H |
| $4-0$ | G2A | Y5 | $\text { O- } \frac{10}{9}$ | H | L | L | H | H | H | H | H | L | H | H | H | H |
| $\bigcirc$ | G2B | Y6 | $0-\frac{9}{7}$ | H | L | H | L | L | H | H | H | H | L | H | H | H |
|  |  |  |  | H | L | H | L | H | H | H | H | H | H | L | H | H |
|  |  |  |  | H | L | H | H | L | H | H | H | H | H | H | L | H |
|  |  |  |  | H | L | H | H | H | H | H | H | H | H | H | H | L |

Nota 1: G2 = G2A + G2B

