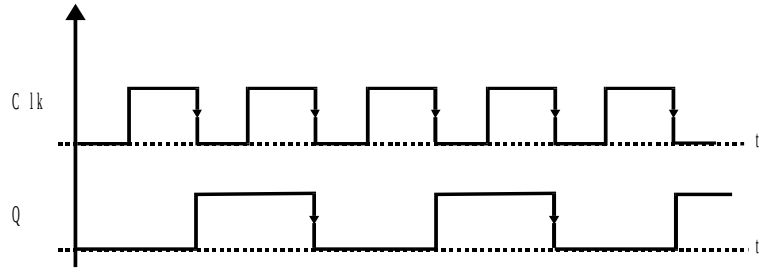
Sequential Systems Exercises

Exercise 1:

Let X be a 3-bits number. Design a circuit that sets a JK flip-flop to “1” when X contains an odd number of “1” and to “0” otherwise.

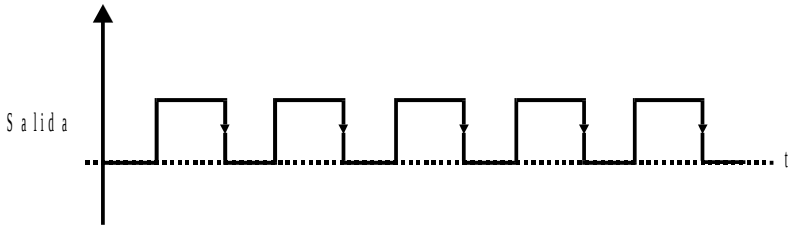
Exercise 2:

Identify the type of latch or flip-flop that has produced this time diagram -chronogram- as output.



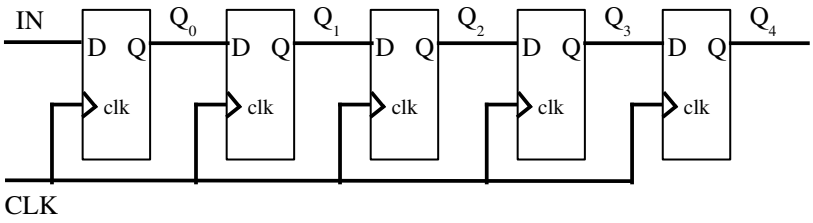
Exercise 3:

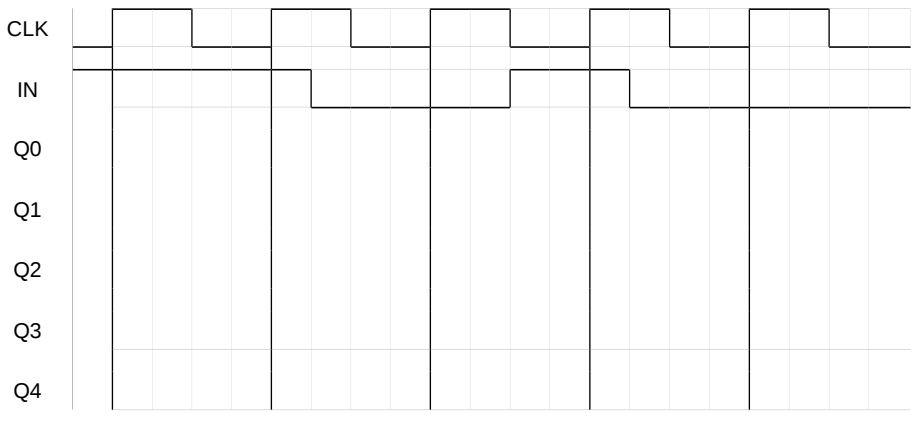
Design a 1/4 frequency divider that produces the following time diagram as output.



Exercise 4:

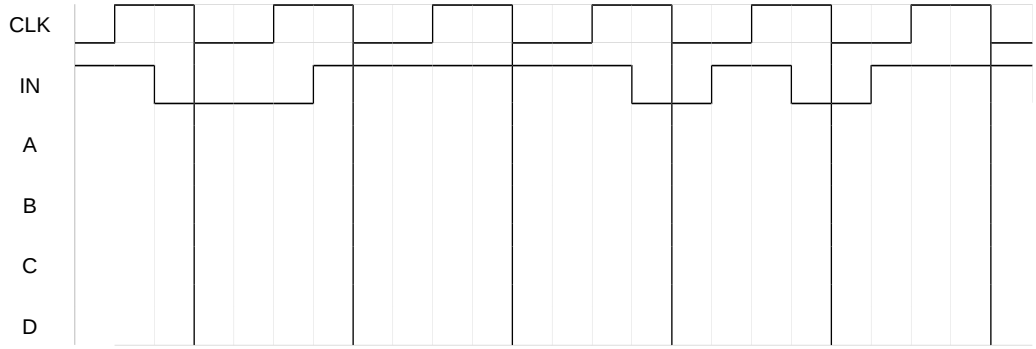
Knowing the inputs CLK and IN of a 5-bits register that initially is in the “00000” state, fill the following chronogram with the time evolution of (Q0-Q4)





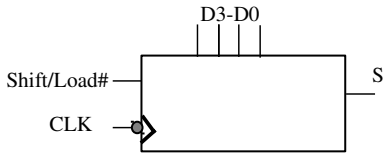
Exercise 5:

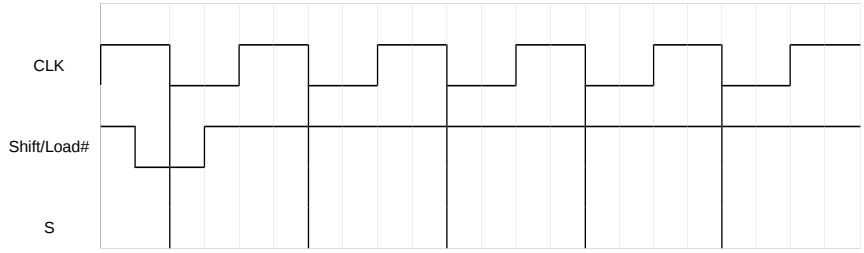
Deduce the four parallel outputs (A-D) of a shift-register made with 4 falling edge-triggered D-latches when the serial input IN is the one shown in the following chronogram. Which data will be obtained after 6 clock cycles?



Exercise 6:

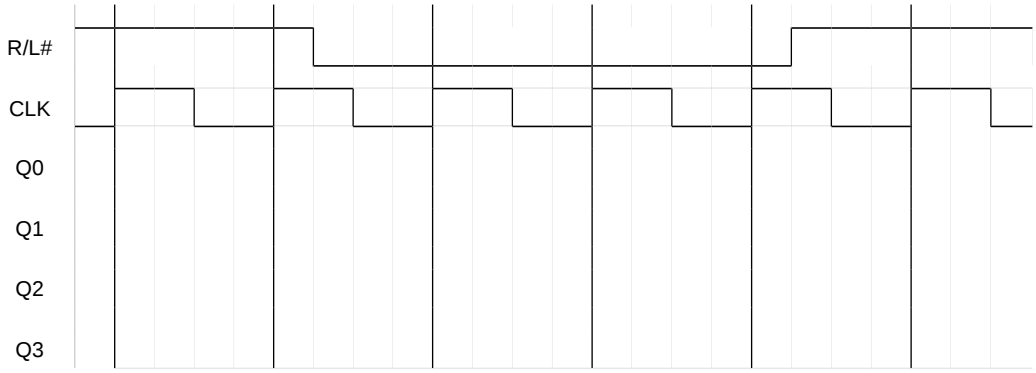
Assuming that the following chronogram corresponds to a parallel input / serial output shift-register, deduce the value of the serial output S in each cycle when the inputs D3-D0 are 1010, and the Shift/Load# signal takes the shown values.





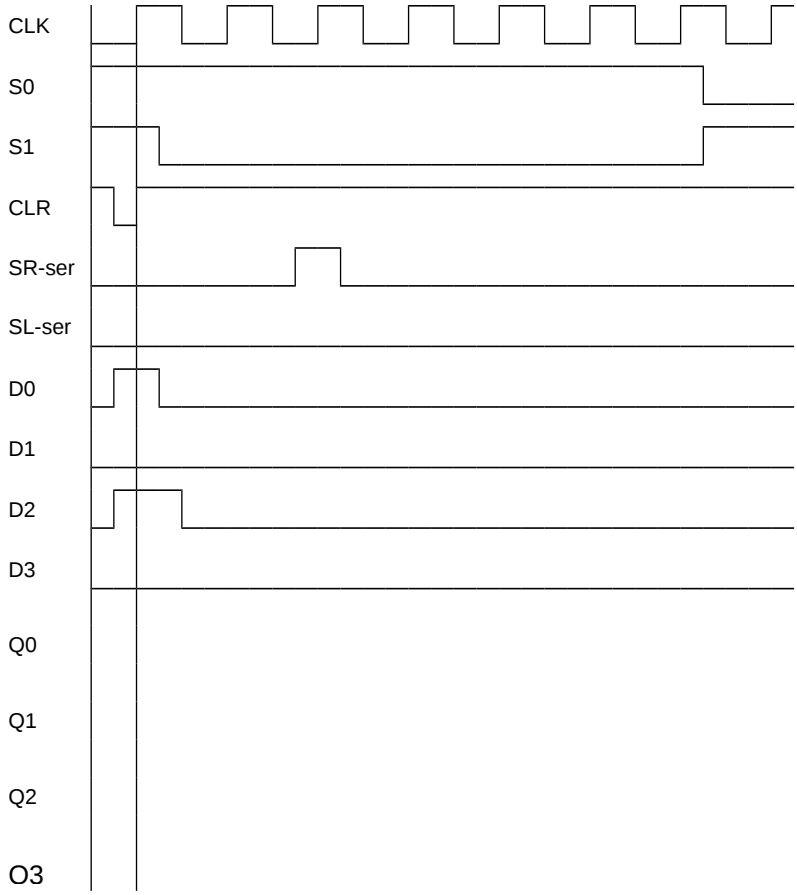
Exercise 7:

Suppose that the following time diagram corresponds to a bidirectional shift register in which the serial input is in LOW level and the indicated control input RIGHT/LEFT# is applied. Deduce the state of the register in each cycle if its initial value is Q0-Q3 = 1101 and the synchronization is with the rising edge of the clock.



Exercise 8:

Deduce state Q0-Q4 of a universal shift register when the shown inputs are applied. Assume that the synchronization is with the rising edge of the clock, that the only non-synchronous signal is CLR, and that the control inputs S0-S1 work as follows: (S0, S1)=(1,1) parallel load; (0,0) no change; (0,1) left-shift, and (1,0) right-shift. SR-ser and SL-ser are the Shift-Right and Shift-Left serial inputs respectively.



Exercise 9:

Design an asynchronous up counter from 2 to 12 with JK flip-flops.

Exercise 10:

Design an asynchronous down counter from 15 to 3 with JK flip-flops.

Exercise 11:

Design an synchronous up counter from 0 to 3 with D flip-flops.

Exercise 12:

Design an synchronous up/down counter from 0 to 7 with J-K flip-flops.

Exercise 13:

Design a synchronous down counter from 5 to 0 with D flip-flops. If the counter is in a state other than 5 to 0, it must go to 0 in the next clock pulse.

Exercise 14:

Design a synchronous counter with JK flip-flops that follows the sequence 1,4,2,7.

Exercise 15:

Design a synchronous counter with D flip-flops and with JK flip-flops that follows the sequence 0,1,3,2,6,7,5,4.

Exercise 16:

Design a circuit with JK flip-flops that detects in the input X the sequence “101” setting the output Z to 1.

Exercise 17:

Design a circuit with D flip-flops that detects in the input X four consecutive “1” setting the output Z to 1.

Exercise 18:

Design a circuit with an input X and an output Y that must take the value “1” whenever the last two bits in the input are equal, and “0” otherwise.